

A K-BAND MONOLITHIC CPW OSCILLATOR CO-INTEGRATED WITH A BUFFER AMPLIFIER

K. Maruhashi, M. Madihian*, L. Desclos*, K. Onda, and M. Kuzuhara

NEC Corporation

Kansai Electronics Res. Lab., 2-9-1, Seiran, Otsu, Shiga 520 Japan

*C&C Res. Labs., 4-1-1, Miyazaki, Miyamae-ku, Kawasaki 216 Japan

Abstract

This paper describes the design approach, fabrication process, and performance of a monolithic CPW oscillator incorporating a buffer amplifier on the same chip, for K-band wireless network applications. At 21GHz, the output power of the oscillator recorded 17dBm with an overall dc-RF efficiency of 22%. By changing the length of a source feedback line, the oscillation frequency was varied up to 26GHz. For all cases, the output power remained higher than 16dBm.

I Introduction

Increasing demand for K- and V-band wireless communication systems[1][2] has stimulated development of small-size local oscillators operating at these frequency bands with a sufficiently high output power to drive RX/TX modules in a transceiver. Heterojunction FET(HJFET) technology permits co-integration of all transceiver elements on the same chip and, thus, promises overall system chip size reduction. Since the output power level of an oscillator is limited[3]-[6] and decreases with increasing frequency, buffer amplifiers can be co-integrated with oscillators to enhance the output power. Application of a buffer amplifier will also help to improve the overall dc-RF efficiency and frequency-pulling characteristics of the oscillator.

Recently reported attempts to develop a monolithic oscillator incorporating a buffer amplifier on the same chip include an 11GHz MESFET oscillator with 17dBm output power and 20% efficiency[7],

and a Q-band MESFET VCO with 19.7dBm and 7% efficiency[8]. To fulfill above requirement for the K-band wireless systems, the present paper describes a small-size high power high efficiency K-band MMIC oscillator by incorporating a single-stage buffer amplifier on the same chip, which provides 17dBm output power with 22% efficiency.

II Circuit Design

A. Oscillator

An equivalent circuit for the K-band CPW oscillator with the buffer amplifier is shown in Fig. 1. The devices for both the oscillator and the buffer amplifier are $0.15\mu m \times 200\mu m$ AlGaAs/InGaAs HJFETs. The oscillator has a series feedback topology. A capacitive CPW stub is connected to the source terminal of the FET as a feedback element. This stub also determines the oscillation frequency.

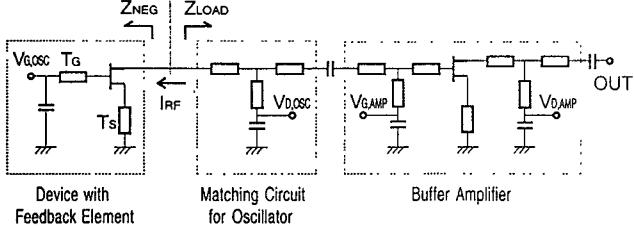


Fig. 1. Equivalent circuit for the K-Band monolithic oscillator incorporating a buffer amplifier.

In the oscillator design, the length of the capacitive and inductive CPW lines (T_S, T_G), which were

connected to the source and gate terminals of the FET, respectively, were determined using a graphical method to get maximum output power as follows. On a harmonic balance simulator, external RF power at a desired oscillation frequency causes an RF current, I_{RF} , into drain terminal of the FET. Using negative resistance at the drain terminal, Z_{NEG} , the oscillation output power, P_{OUT} , can be calculated as $P_{OUT} = -\text{Re}(Z_{NEG}) I_{RF}^2$, when the matching circuit is connected to the drain port so that its impedance, Z_{LOAD} , is equal to $-Z_{NEG}$. For a given I_{RF} , optimum combination of T_S and T_G can be found to get the maximum P_{OUT} at the desired frequency (see Fig. 2). This method provides a direct understanding of the relationship between circuit parameters such as T_S and T_G , and the output power. Thus, a fast optimization without an iteration process is realized. In the design, we avoided the edge of the non-oscillating region in Fig. 2, so that small changes in the device parameters would not stop oscillation. The matching circuit for the oscillator was designed to transform Z_{LOAD} into a 50Ω load.

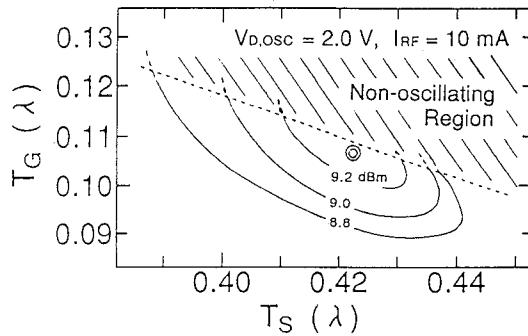


Fig. 2. Calculated oscillator output power as a function of CPW line lengths(T_S, T_G) for RF current(I_{RF})=10mA at 24GHz (without a buffer amplifier).

B. Buffer Amplifier

The amplifier was designed to operate at a center frequency of 24GHz. To insure the stability of the amplifier, a CPW inductive feedback was connected to the source terminal of the FET. Applying a large-signal harmonic balance method, the matching circuits and the length of the feedback line were optimized so as to make the amplifier operate near the saturation output with a high gain. Both the input and output ports of the amplifier were matched

to a 50Ω impedance.

III Fabrication Process and Device Characteristics

The K-band oscillator with the buffer amplifier was fabricated on a 3-inch GaAs substrate. Fig. 3 shows a cross-sectional view for a step-doped AlGaAs/InGaAs HJFET used in the MMIC. The epitaxial layer structure consists of an AlGaAs/GaAs superlattice followed by GaAs and AlGaAs buffers, a 13nm $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ channel, a step-doped($1 \times 10^{18}\text{cm}^{-3}$ / $3 \times 10^{18}\text{cm}^{-3}$) 40nm $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$, and an 80nm n^+ -GaAs cap layer doped $3 \times 10^{18}\text{cm}^{-3}$. In the FET fabrication process, mesa-isolation, conventional photo-lithography, electron beam evaporation and lift-off techniques have been employed. Details have been reported elsewhere[9][10]. A Metal-Insulator-Metal(MIM) structure with SiN film as a dielectric layer was applied for fabricating both dc blocking and bypass capacitors. The CPW structure utilizes a $2\text{-}\mu\text{m}$ thick Au-plated layer.

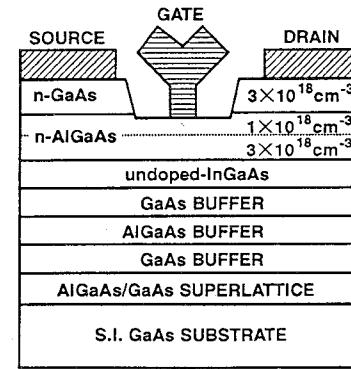


Fig. 3. Cross-sectional view for a step-doped AlGaAs/InGaAs HJFET.

The HJFET has a gate length of $0.15\mu\text{m}$ and a total gate width of $200\mu\text{m}$ ($25\mu\text{m} \times 8$). The device has a typical transconductance of 380mS/mm and an f_T of 70GHz both at a drain bias of 2V with a reverse gate-drain breakdown voltage of 11V . Measured minimum noise figure for the device is 1.1dB at 24GHz with an associated gain of 9.5dB .

IV Performances

Fig.4 shows a chip photograph for the fabricated K-band CPW oscillator with the buffer amplifier. The MMIC chip size is $2.22\text{mm} \times 1.07\text{mm} \times 0.26\text{mm}$.

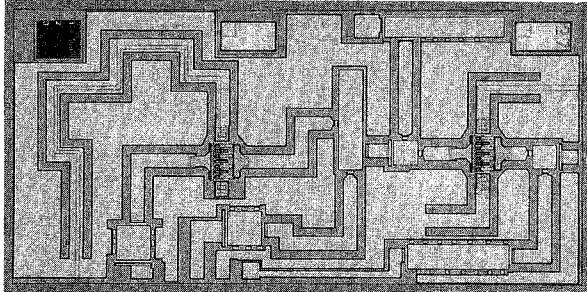


Fig. 4. Chip photograph of the K-band CPW oscillator incorporating a buffer amplifier ($2.22 \times 1.07\text{mm}^2$).

Three different oscillators were developed by changing the length of the 50Ω line, T_S , as 0.43λ , 0.41λ , and 0.38λ , which resulted in oscillation at around 21GHz, 24GHz, and 26GHz, respectively. In the above expressions, λ is the wavelength of each line at 24GHz.

Output power, oscillation frequency, and efficiency as a function of the amplifier drain voltage, $V_{D,AMP}$, for the case of the 24GHz oscillator is shown in Fig. 5. For oscillator gate voltage, $V_{G,OSC} = -0.57\text{V}$, drain voltage, $V_{D,OSC} = 2.0\text{V}$, and amplifier gate voltage, $V_{G,AMP} = -0.42\text{V}$, the output power increased with $V_{D,AMP}$, and reached a maximum value of 14dBm at $V_{D,AMP} = 3.0\text{V}$. The overall dc-RF efficiency took its maximum value of 17% at around $V_{D,AMP} = 2.0\text{V}$. On the other hand, the oscillation frequency shifted only 160MHz when $V_{D,AMP}$ was varied from 0.5V to 3.0V.

Fig.6 shows the maximum output power of each oscillator at $V_{D,OSC} = V_{D,AMP} = 2.0\text{V}$ and $V_{D,OSC} = V_{D,AMP} = 3.0\text{V}$. When the bias voltage was increased from 2V to 3V, the output power increased by about 4dB. For all oscillators, the output power was higher than 16dBm. The 21GHz oscillator output power was 17dBm with an overall dc-RF efficiency of 22% at $V_{D,OSC} = V_{D,AMP} = 3.0\text{V}$.

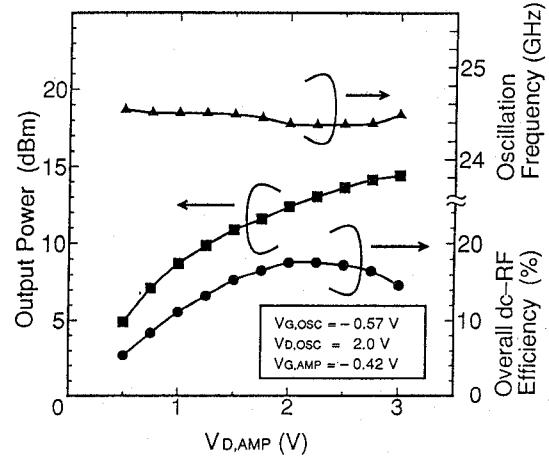


Fig. 5. Output power, oscillation frequency, and overall dc-RF efficiency as a function of amplifier drain voltage ($V_{D,AMP}$).

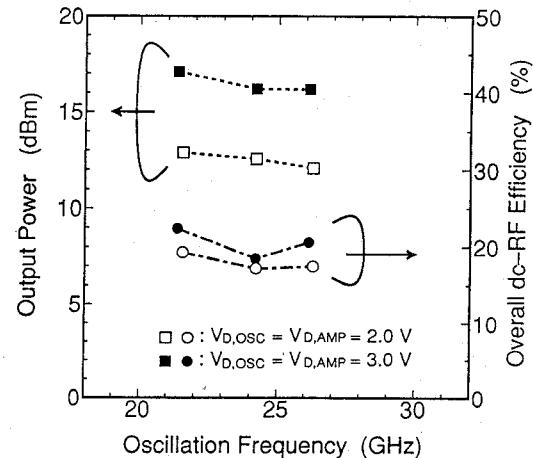


Fig. 6. Maximum output power for each oscillator and overall dc-RF efficiency at $V_{D,OSC} = V_{D,AMP} = 2.0\text{V}$ and $V_{D,OSC} = V_{D,AMP} = 3.0\text{V}$.

V Conclusions

The design approach, fabrication process, and performance of a K-band MMIC oscillator incorporating a buffer amplifier on a single chip were described. By changing the length of the source feedback line, the oscillation frequency was varied from 21GHz to 26GHz. For all cases, the output power was higher than 16dBm. At 21GHz, the output

power of the oscillator recorded 17dBm with an overall dc-RF efficiency of 22%.

Since the output power of the developed MMIC oscillators is considerably high, they can directly drive mixers in transmitter/receiver modules with no additional power amplification.

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